Sub-Micron Gate FET's by Optical Lithography Using Re-flow and SOG Method

W.-S. Lour, M.-K. Tsai*, K.-C. Chen, Y.-W. Wu, S.-W. Tan and Y.-J. Yang*
Dept. of E.E., National Taiwan-Ocean University,
2, Peining Road, Keelung, Taiwan, Republic of China.
*Dept. of E.E., National Taiwan University,
1, Sec. 4, Roosevelt Road, Taipei, Taiwan, R. O. C.

GaAs ICs are taking the roads in record numbers. There numerous application and business opportunities in the wireless telecommunication, data transmission, high speed networking. In particular, PHEMT has its performance advantage over its rival (HBT) in term of operation voltage [1-2]. Basically, the present widely used line width for GaAs-based FET's is 0.5 μm. However, it is difficult to accomplish such a fine line by conventional optical lithography (in particular for G- and I-line aligners). On the other hand, to reduce the RC delay time for high-speed performance, a thick gate-metal deposition is demanded for low parasitic resistance. This is another challenge for conventional optical lithographic.

In this presentation, we will report a novel sub-micron gate FET processing technique, in which conventional optical aligner was employed to implement a 0.2~0.7 μm gate length. The key features of the new methodology include 1) the use of spin on glass and 2) line width controlled by photo-resist (PR) re-flow. We obtained sub-micron undercut windows from micron-level patterned PR. They are very promising for depositing fine-line gate metal with low parasitic resistance.

To realize the novel processing steps in fabricating sub-micron gate FET's, we refer to the inset in Fig. 1(b). After finishing the required device isolation, ohmic drain/source contact, multiple SOG (spin-on-glass) was deposited on the whole wafer and cured at various temperatures. Forming micron-level PR patterns on the gate area and then performing PR re-flow. As shown in Fig. 1(a) the extension width of PR (ΔL) as a function of re-flow time. The used re-flow time is five minutes. The measured ΔL is 0.1 μm increasing to 0.3 μm as the used temperature is 100 to 160 ^{o}C. In contrast, Fig. 1(b) shows the relation between extension width an re-flow time, where the re-flow temperature of 120 ^{o}C is used as a parameter. According to the experimental results one can well control the required gate dimension by appropriately choosing the re-flow temperature and re-flow time. In facts, we have successfully fabricated 0.2- to 0.8-μm gate metals from 0.8- to 1.2-μm PR patterns.

Fig. 2 shows the SEM picture obtained after PR patterning and re-flowing. The baseline parameters used are 1.2-μm PR initial pattern, 130- ^{o}C re-flow temperature, 5-minute re-flow time, and the final pattern is 0.8 μm.

Fig. 3 is an SEM picture illustrating a gate of 0.6 μm fabricated by defining a 1.2 μm PR pattern. The authors will further report the detailed data and description of PR re-flow as well as how to form etched SOG with nice undercut (just shown in the figure). These are key characteristics in obtaining high yield FET's with sub-micron gate by conventional optical lithographic. At last, HEMT's fabricated by this new technique will also be reported here.

ACKNOWLEDGEMENTS

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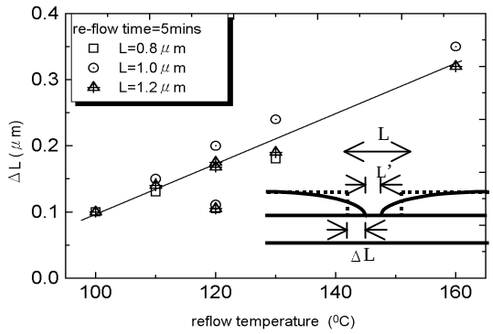

Fig. 1(a): the extension width of PR (ΔL) as a function of re-flow time.

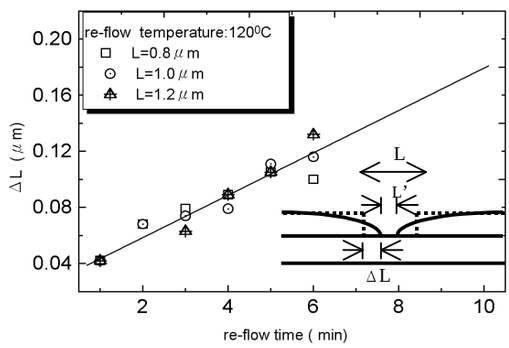

Fig. 1(b): the relation between extension width an re-flow time, where the re-flow temperature of 120 ^{o}C is used as a parameter.

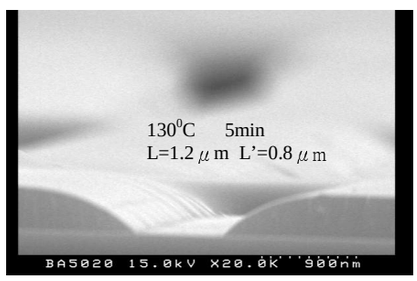

Fig. 2: the SEM picture obtained after PR patterning and re-flowing.

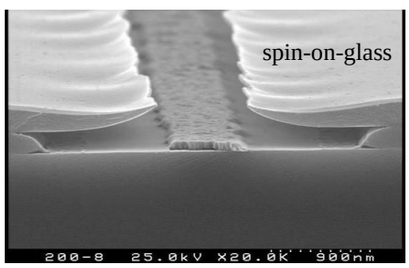

Fig. 3: the SEM picture illustrating a gate of 0.6 μm fabricated by defining a 1.2 μm PR pattern.